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GeodeLink™ System Architecture for National Semiconductor's Information Appliances Technology

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GeodeLink™

- Current Information Appliance system architectures
- GeodeLink™ system architecture for IA
  - Interconnect architecture
  - GeodeLink interface unit
  - GeodeLink memory controller
  - x86 and PCI Compatible SW Model
  - Active hardware power management
  - Development support

Information Appliance Space

- Requires optimization of not just the CPU
- The entire system must be optimal
  - Low cost
  - Low power
  - Optimal performance
  - SW compatibility
- Requires high levels of integration and complexity
  - Reduce cost, reduce power, increase performance
- Natural evolution of the PC

Set-Top Box

Personal Access Device

Thin Client

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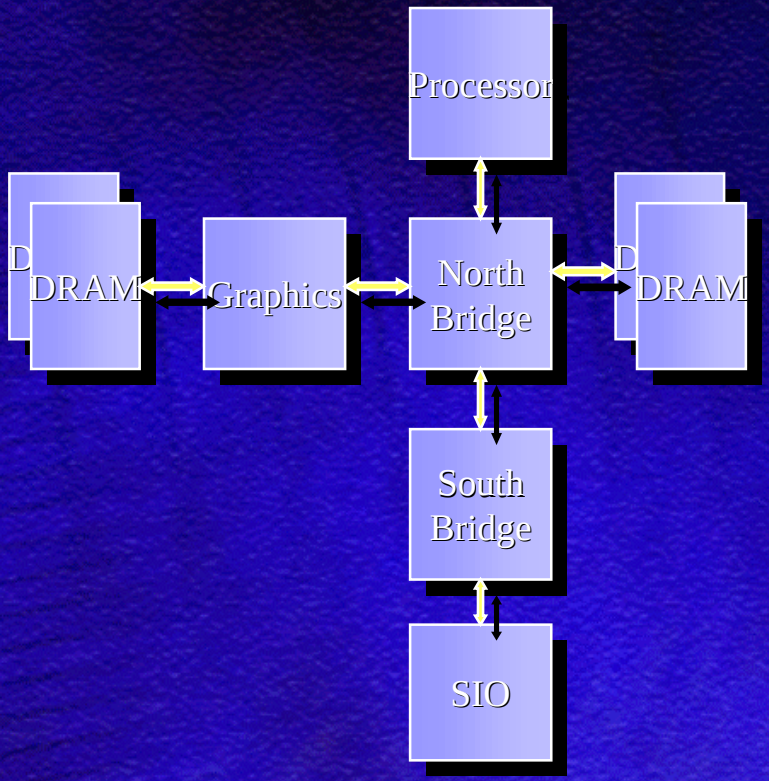
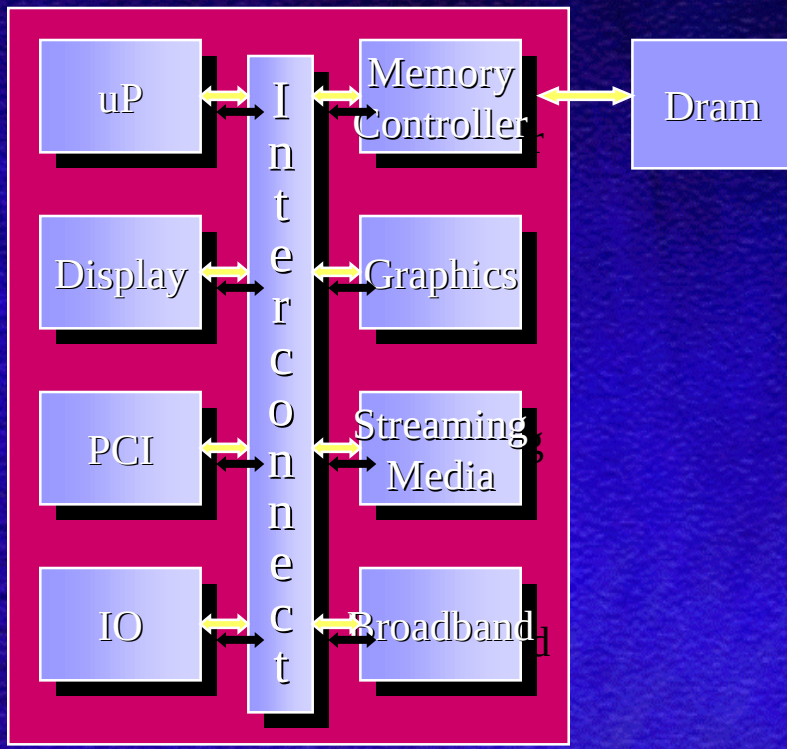
Evolution of the PC

- Multiple bus interfaces for modular systems
- Multiple memory interfaces
- Optimal cost/performance for PC
- Optimized for the CPU Mhz treadmill
- Optimized for the graphics processor feature treadmill
- Bridging increases latency, limits bandwidth and consumes power



Integrated Information Appliance

- **Pros**
  - **Reduce package cost**
  - **Reduce I/f power**
  - **Increase performance**
  - **Minimize latency**
- **Cons**
  - **Complex verification**
  - **Mixed traffic types**
  - **Complex system interaction**
  - **New SW model**



IA Customers needed ...

- Revolutionized system architecture for information appliances
  - High performance on chip interconnect
  - Mixed unrelated system components without unexpected system effects
- Existing SW model preserved
- Additional SW/HW features
  - Debug with high level integration
  - Power management for IA

GeodeLink™ Is the Industry's FIRST IA System Architecture

GeodeLink™ Is a Top to Bottom System Architecture for Information Appliance System-On-a-Chip

- **High Performance On-chip Interconnect**
- **Optimized Unified Memory Architecture (UMA)**
- **Standard GeodeLink™ Software Model**
  - **Virtual PCI System Architecture**
  - **X86 Compatible**
  - **Retains Existing Software Models**
  - **Active Hardware Power Management**
- **On-chip Development Support**

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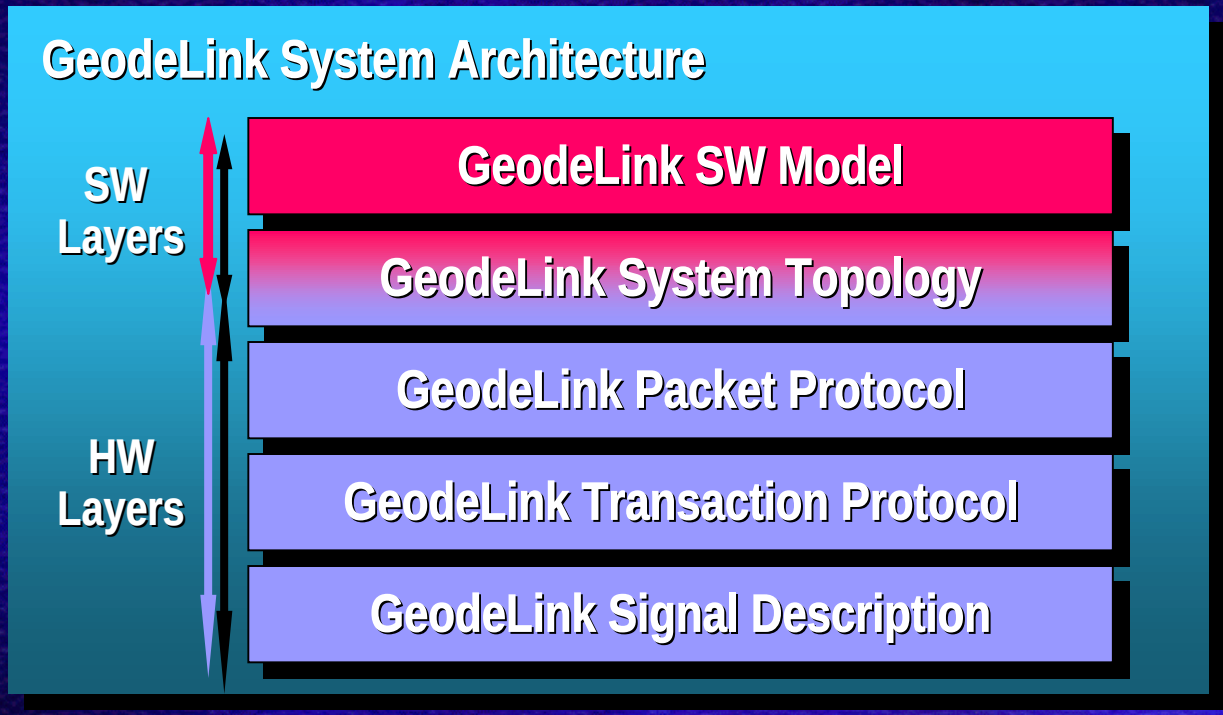
GeodeLink™ System Architecture

PCI System Architecture

X86 SW

Development Tools



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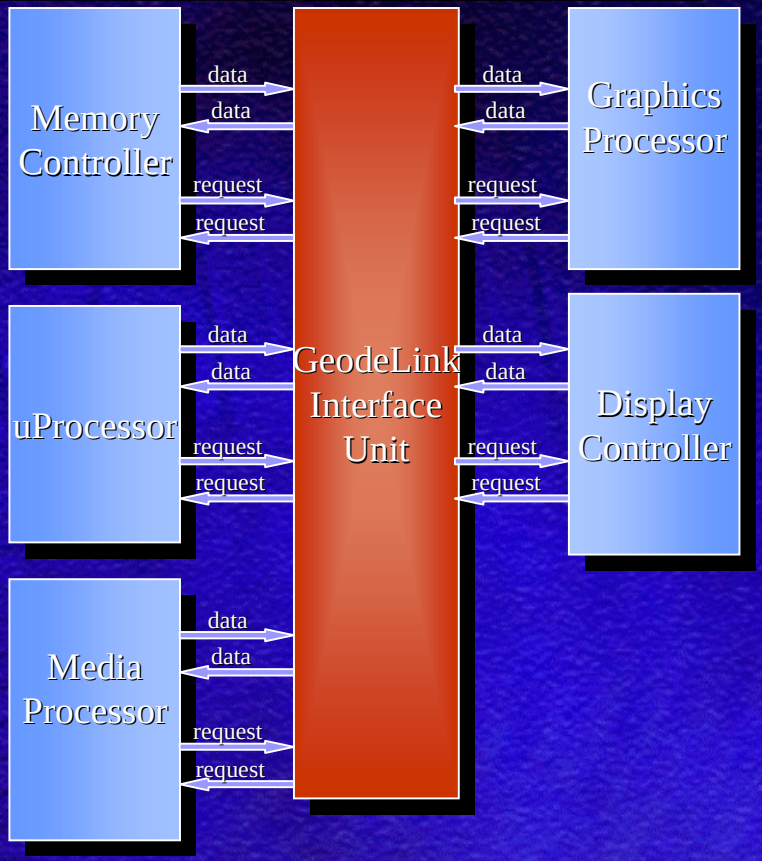
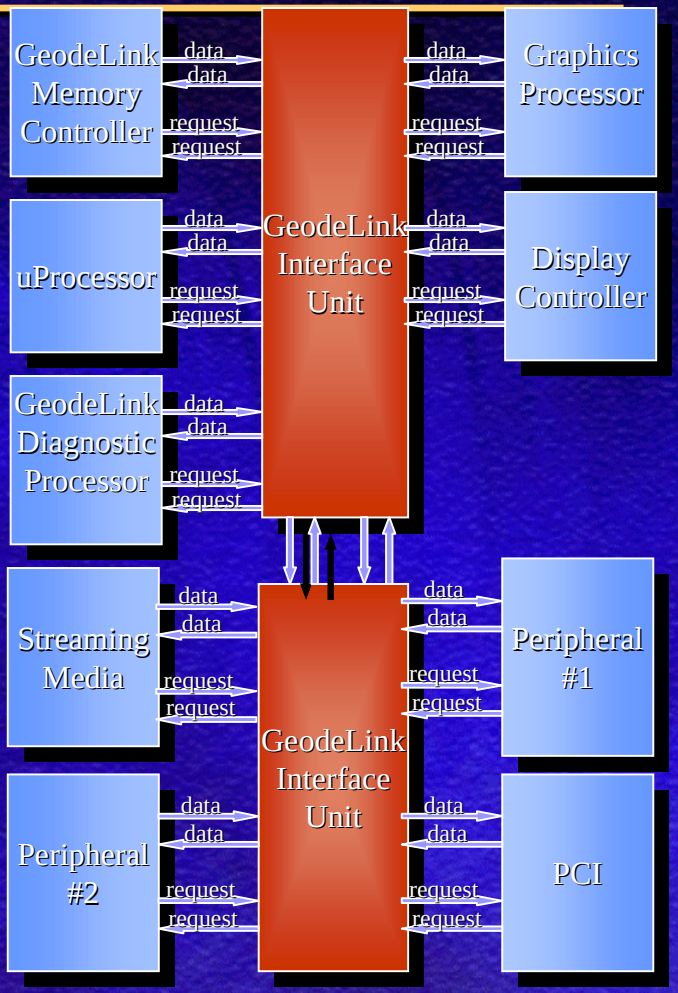
GeodeLink™ Interconnect

- Remove the interconnect bottlenecks
  - Put everything on 1 chip
  - Low latency access for latency critical devices
  - Source and sink equal BW
- Independent data and request buses
- Non-blocking multiple masters
- Deep pipelining and split transactions
- Peer to Peer transactions for streaming media



GeodeLink™ Interconnect

- No centralized bus
  - Multiple hierarchical hubs and spokes
  - Multiple GeodeLink interface units
- Each device has a private link to the interconnect
- Out of order data streams
- Closed loop write completion
- The interconnect is never the bottleneck!



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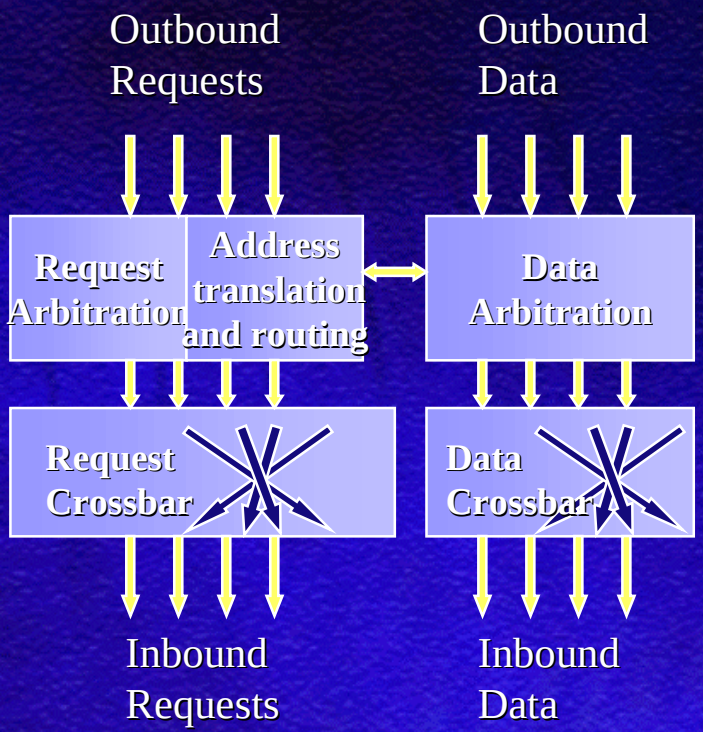
GeodeLink™ Interface Unit

- Smart Crossbar Interconnect Fabric
- Multiple simultaneous active master
- Address are translated and routed for physical to physical mapping
- Interfaces are unidirectional and fully synchronous
- 31 outstanding transactions/device



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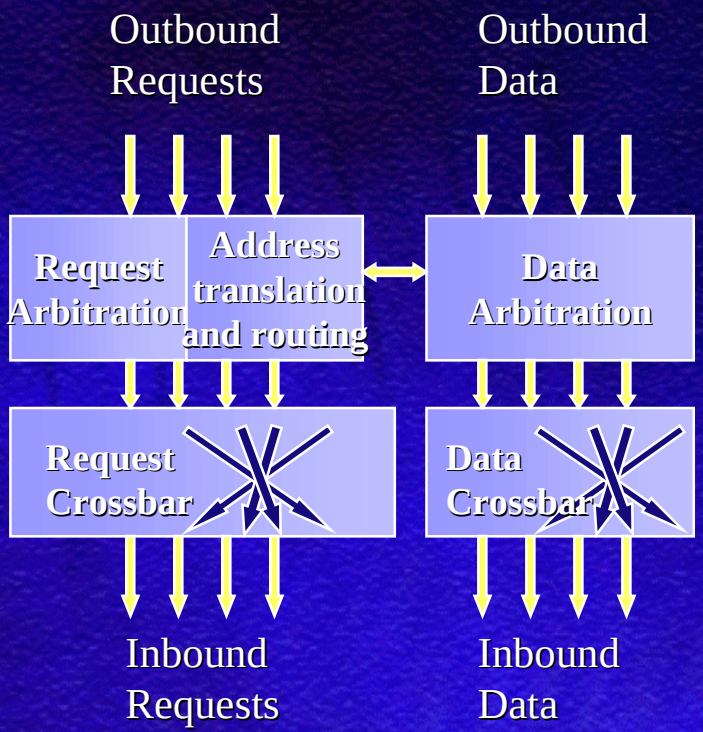
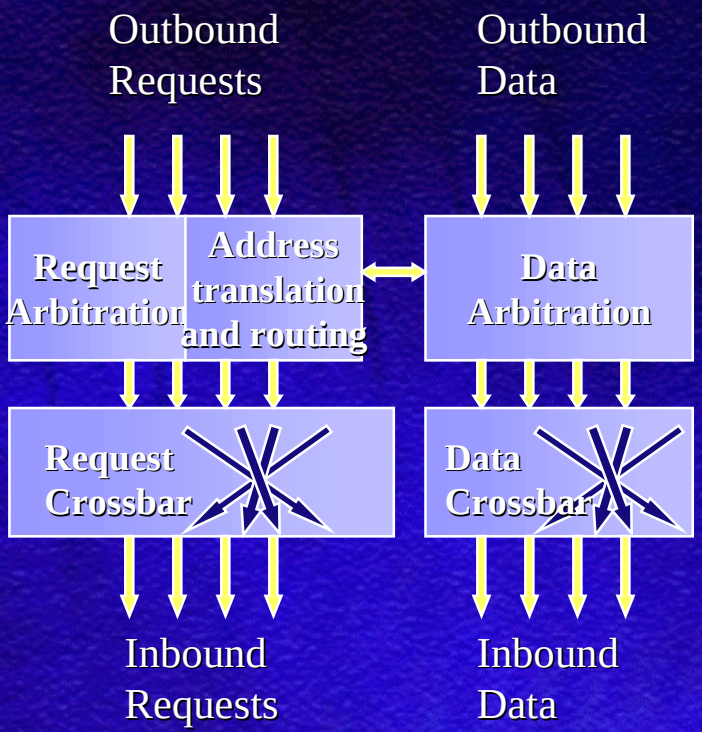
GeodeLink™ Interface Unit

- **Smart Crossbar Interconnect Rates**
  - **2 arbitrated requests/clk**
  - **3 arbitrated data transfers/clk**
  - **extendable to 7 req/clk, 7 data/clk**
  - **example 64 bit @ 266 MHz**
    - **Request rate = 533 Mreq/s**
    - **Data rate = 6 GB/s**
- **Out of order data return for optimal request ordering**
- **Speculative arbitration for fast request routing**



GeodeLink™ Interface Unit

- 8 independent streams per device
- Streams dynamically manage their priority
  - Devices change priorities per/request
  - Entire data stream inherits the current priority
- GeodeLink Interface Unit maintains all ordering, hazard detection and interlocks



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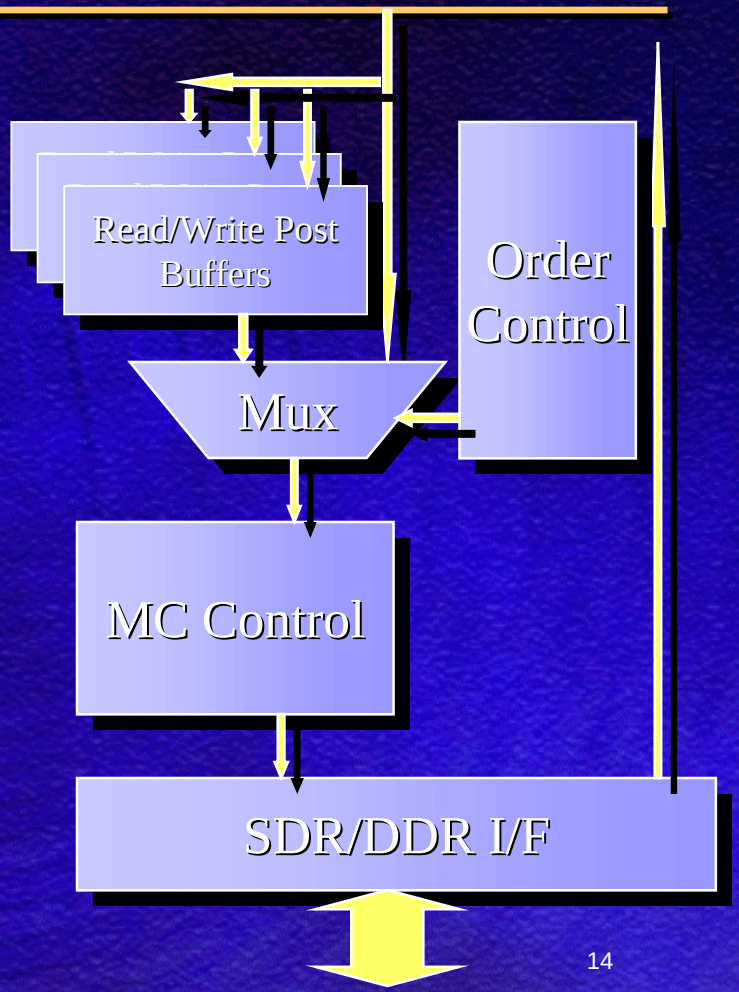
GeodeLink™ Memory Controller

- Optimized for UMA arbitration
  - Each data stream is in order
  - Multiple data streams are out of order
  - Dynamic priority elevation
  - Up to 64 data streams
- Read forwarding around writes
- Open page forwarding around closed page (latency tolerant streams)
- SDR or DDR SDRAM
- 32 or 64 bit interface
- 66-266MHz data rates
  - Up to 2GB/s peak BW



GeodeLink™ SW Model

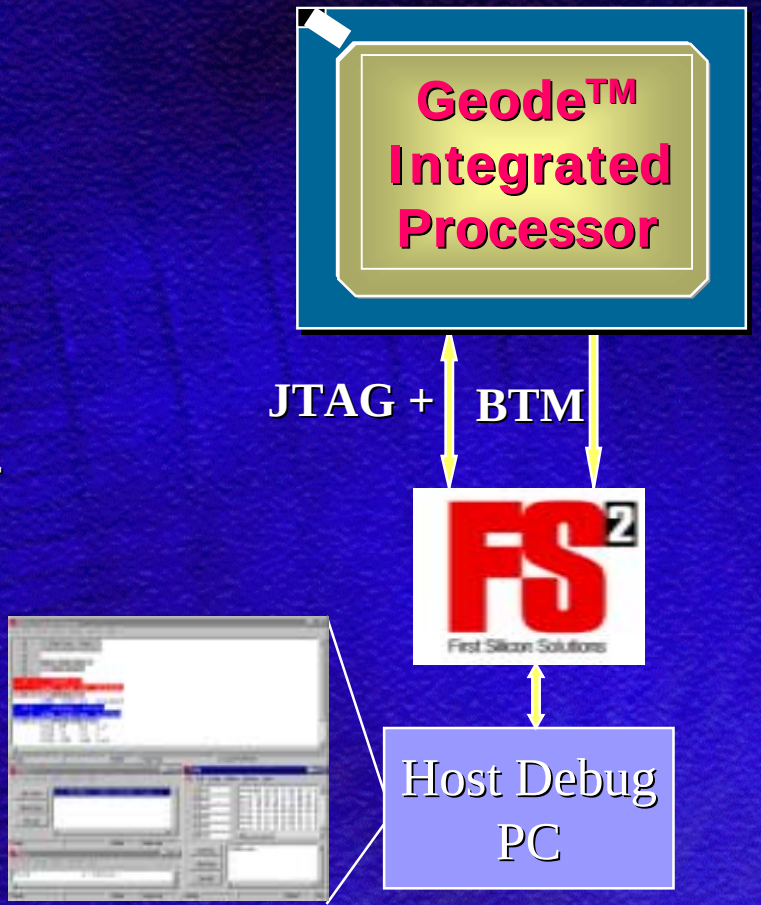
- Optimized crossbar interconnect requires a non-standard bus architecture
- Virtual PCI system architecture
  - GeodeLink appears to SW like a PCI system architecture
  - Legacy PCI device drivers work on GeodeLink devices
- Compatible with x86 systems
- Maximizes SW compatibility with future National products and existing systems

GeodeLink™ SW Model: Active Hardware Power Management

- IA PM is much more than uP PM
- No standard power management model for Information appliances
- SW transparent, transaction based power management
- Compatible with ACPI and APM when available
- For non ACPI or APM compatible OS
  - AHPM provides a complete PM solution underneath the OS via System Management Mode
  - Actively manages power without OS interaction
  - Support customer modifications and extensions via plug in extensions

GeodeLink™ Development Environment

- FS2
  - branch trace messaging decode
  - JTAG interface HW/SW
  - TCL front end
  - Stop on clock
  - CPU and peripheral triggers
- Interfaces with common 3rd party debugger
- JTAG provides full bus master access
  - Register/io/mem rd/wr
  - Processor and peripheral state
  - Serial scan chain access
- Extended x86 debug registers



Summary

- GeodeLink™ optimized for high performance UMA
- Optimized for minimal bottlenecks, low latency, and streaming multimedia
- High levels integration == cost & power savings
- Uses industry standard x86 and PCI SW models
- Provides standard HW power management
- Enables customer development environment
- Allows 3rd parties to innovate for National's IP
- Products based on GeodeLink architecture available in 1H02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